WHAT IS CLAIMED IS:

1. A data storage device comprising:

a first memory cell string that includes at least a first magnetic random access memory (MRAM) cell coupled to a second MRAM cell; and

a circuit coupled to a node between the first MRAM cell and the second MRAM cell, the circuit configured to detect a voltage change at the node in response to a voltage being provided to the memory cell string and in response to a write sense current being applied across the first MRAM cell.

2. The data storage device of claim 1 wherein the circuit is configured to detect that the first MRAM cell was in a first state in response to detecting the voltage change.

3. The data storage device of claim 2 wherein the circuit is configured to cause a logic level associated with the first state to be read out.

4. The data storage device of claim 2 wherein the circuit is configured to detect that the first MRAM cell was in a second state in response to not detecting the voltage change.

5. The data storage device of claim 4 wherein the circuit is configured to cause a logic level associated with the second state to be read out.

6. The data storage device of claim 1 wherein the first memory cell string has a first end and a second end, wherein the voltage is provided to the first end, and wherein the second end is coupled to a ground source.

7. The data storage device of claim 6 further comprising:

a second memory cell string that includes a third MRAM cell coupled to a fourth MRAM cell; and

wherein the second memory cell string has a third end and a fourth end, and wherein the third end and the fourth end are coupled to the ground source in response to the write sense current being applied across the first MRAM cell.

8. The data storage device of claim 6 wherein the first MRAM cell is coupled to the first end, and wherein the second MRAM cell is coupled to the second end.

9. The data storage device of claim 6 wherein the first MRAM cell is coupled to the second end, and wherein the second MRAM cell is coupled to the first end.

10. The data storage device of claim 6 wherein the memory cell string includes a third MRAM cell and a fourth MRAM cell, and wherein the first, the second, the third, and the fourth MRAM cells are coupled in series.

11. The data storage device of claim 1 wherein the first MRAM cell comprises a data layer and a reference layer, wherein the write sense current sets the reference layer to a first state, and wherein the write sense current does not change a second state of the data layer.

12. A method of performing a read operation from a first memory cell in a memory cell string that includes the first memory cell and a second memory cell comprising:

providing a voltage to the memory cell string;

measuring a first voltage at a node between the first and second memory cells;

applying a write sense current across the first memory cell;

measuring a second voltage at the node; and

determining whether the first voltage differs from the second voltage.

13. The method of claim 12 further comprising:

determining that the first memory cell was in a first state in response to the first voltage differing from the second voltage.

14. The method of claim 13 further comprising:

reading out a logic level associated with the first state in response to the first voltage differing from the second voltage.

15. The method of claim 13 further comprising:

determining that the first memory cell was in a second state in response to the first voltage not differing from the second voltage.

16. The method of claim 15 further comprising:

reading out a logic level associated with the second state in response to the first voltage not differing from the second voltage.

17. The method of claim 12 further comprising:

applying the write sense current across the first memory cell to set a reference layer of the first memory cell to a known state.

18. A system comprising:

a first memory cell;

a second memory cell coupled to the first memory cell;

a transistor coupled to a node between the first and second memory cells and coupled to a bit line associated with the first memory cell;

a means coupled to the bit line for detecting a voltage change at the node in response to:

a first voltage being provided to the first and second memory cells;

a write sense current being applied on the bit line; and

a second voltage being provided to the transistor.

19. The system of claim 18 wherein the transistor comprises a voltage follower transistor.

20. The system of claim 18 wherein the transistor includes a gate connection, a source connection, and a drain connection, wherein the gate connection is coupled to the node, and wherein the source connection is coupled to the bit line.

21. The system of claim 18 wherein the transistor includes a gate connection, a source connection, and a drain connection, wherein the source connection is coupled to the node, and wherein the drain connection is coupled to the bit line.

22. The system of claim 18 wherein the transistor includes a gate connection, a source connection, and a drain connection, wherein the drain connection is coupled to the node, and wherein the source connection is coupled to the bit line.

23. The system of claim 18 wherein means is for detecting that the first memory cell was in a first state in response to detecting the voltage change, and wherein the means is for causing a first logic level associated with the first state to be read out.

24. The system of claim 23 wherein the means is for detecting that the first memory cell was in a second state in response to not detecting the voltage change, and wherein the means is for causing a second logic level associated with the second state to be read out.

25. The system of claim 18 a voltage source configured to provide the first voltage and the second voltage.